wherein the layer of first material is formed such that the first lower level lies above the wafer upper level by a value that is equal to or greater than the thickness.

21. (Amended) The method of claim 22 wherein the first material is doped polysilicon.

22. (Amended) A method of planarizing a layer of semiconductor material on a processed wafer, the wafer having a top surface, the top surface having a wafer lower level and a wafer upper level that lies above the wafer lower level, the method comprising the steps of:

forming a layer of first material on the top surface of the wafer, the layer of first material having a top surface, the top surface of the layer of first material having a first lower level and a first upper level that lies above the first lower level;

forming a layer of second material on the top surface of the layer of first material; and

chemically-mechanically polishing the layer of second material and the underlying layer of first material until the layer of first material is substantially planar to form a planarized layer of first material, the planarized layer of first material covering the wafer upper level of the top surface of the wafer; and

forming a layer of third material on the planarized layer of first material.

23. (Amended) The method of claim 22 wherein the layer of first material makes an electrical contact with a device on the wafer.